

A complementary metal–oxide–semiconductor anode array chip with two rows of 512 anodes and dual integrated analog read-out circuitry

Dennis Nevejans^{a)} and Eddy Neefs

BIRA-IASB, Belgian Institute for Space Aeronomy, Ringlaan 3, B-1180 Brussels, Belgium

Spyros Kavadias, Patrick Merken, Chris Van Hoof, Giuseppe Gramegna,^{b)} Johan Bastiaens,^{c)} and Bart Dierickx

IMEC, Kapeldreef 75, 3001 Leuven, Belgium

(Received 27 June 2000; accepted for publication 9 August 2000)

A novel multianode electron detector chip (LEDA512) has been designed, fabricated and tested using a 0.7 μm complementary metal–oxide–semiconductor technology. This chip, mounted behind a stack of two microchannel plates, is used in a positive ion mass spectrometer selected by the European Space Agency for the ROSETTA cometary mission. Two functions are integrated on the chip: a dual row of 512 anodes, each having an area of 22 $\mu\text{m} \times 8 \text{ mm}$ for the collection of electrons, and two separate anode multiplexer and charge amplifier units. For redundancy reasons the chip has been designed such that the two anode rows with their associated electronics are identical and may be used independently with separate clocks and power supplies. Tests have confirmed that the LEDA512/microchannel plate combination is working properly as an ion detector and that excellent noise and response may be obtained in combination with the mass spectrometer.

© 2000 American Institute of Physics. [S0034-6748(00)04511-1]

I. INTRODUCTION

In 1993 the Science Program Committee of the European Space Agency approved the ROSETTA mission¹ as the planetary cornerstone mission of its long-term science program. The ROSETTA spacecraft fulfilling this mission is scheduled for launch in 2003 and will perform a rendezvous with comet 46 P/Wirtanen in 2011, after a swingby of planet Mars and two asteroid flybys. One of the instruments selected for this mission is the Rosetta orbiter spectrometer for ion and neutral analysis (ROSINA),² part of which is the double focusing mass spectrometer (DFMS).

During the feasibility study for the ROSINA DFMS magnetic mass spectrometer the need arose for a focal plane ion detector having a large sensitivity range and being capable of recording simultaneously a series of ion mass peaks with high mass resolution. The device described in this article constitutes, in combination with a stack of two microchannel plates (MCPs) mounted in front of it, a focal plane array for the recording of positive ion mass spectra. The adjustable ion to electron conversion gain of the MCP stack realizes the desired variable sensitivity, while the analog charge collection and read-out system in the chip is responsible for the collection of the MCP output charge with high spatial resolution, low noise, and large dynamic range.

In the past, devices capable of position sensitive charged particle detection have been designed and built in many con-

figurations with different working principles. Devices have been implemented as: arrays of discrete anodes connected to individual pulse discriminators/counters,³ charge division or rise-time detectors based on either resistive anode strips⁴ or capacitively coupled anode networks,^{5,6} coincidence event detectors,⁷ a self-scanning electron collector array,⁸ and several other variants.⁹ Only a few detectors fulfill the requirements of combining widely adjustable MCP gain and the simultaneous recording of ion spectra over a wide sensitivity range and high spatial resolution. However, those devices do not comply with requirements like circuit redundancy and on-chip integration of analog read-out electronics. Therefore, a new detector chip was designed in standard complementary metal–oxide–semiconductor (CMOS) technology. The chip integrates two identical but independent detector units, each composed of a row of 512 separate floating anodes, an analog multiplexer addressed by a shift register, a voltage reference, and a charge sensitive amplifier. The chip is named LEDA512, which stands for linear electron detector array with 512 anodes.

In the following paragraphs, the architecture and operation of the chip will be presented followed by some test results. Finally, some other areas of application will be suggested and some conclusions resulting from the present development will be drawn.

II. CHIP DESCRIPTION AND OPERATION

The LEDA512 chip is used for the measurement of ion spectra in a double focusing mass spectrometer. A stack of two MCP devices is mounted in close proximity in front of the chip surface. The MCPs emit an electron cloud each time the front of the stack is hit by an impinging ion. The impact position of this ion is selected by the mass spectrometer ac-

^{a)}Author to whom correspondence should be addressed; electronic mail: Dennis.Nevjans@bira-iasb.oma.be

^{b)}Present address: STMicroelectronics, Str. Primosole 50, 45 100 Catania, Italy.

^{c)}Present address: Monolithic System Technology Inc., 1020 Stewart Drive, Sunnyvale, CA 94086.

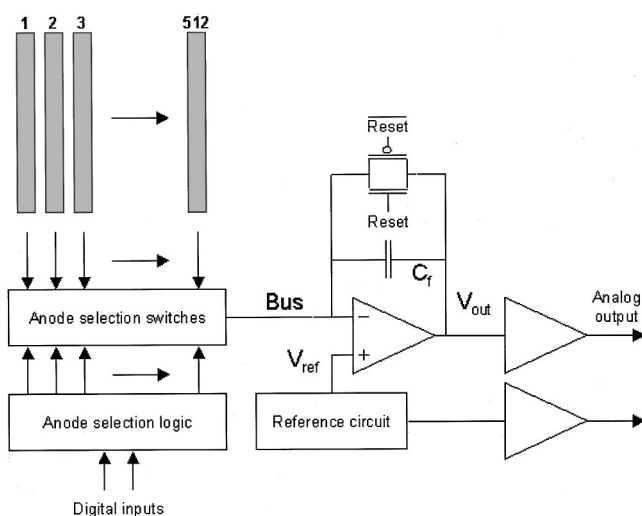


FIG. 1. Block diagram of a half LEDA512 chip.

according to its mass-to-charge ratio. The electrical field applied between the MCP back and the chip guides the electrons produced by the MCP towards the chip. Subsequently, the floating anodes—deposited using the metal layer on top of the CMOS chip—collect these electrons.

A. General architecture and signal read-out

An important requirement for the chip is the capability for redundancy. Since the instrument will be flying on a long duration space mission, detector redundancy was of utmost importance. Therefore, two identical linear anode arrays were implemented, which could be operated with independent power supply voltages, clock, and output signals without influencing each other. In order to obtain arrays with matched characteristics, both were integrated on the same chip in such a way that the layout of both anode arrays and their associated electronics is mirrored with respect to the central axis of the chip. We will therefore only discuss the block diagram of one of the two identical subunits.

The building blocks of the chip are shown in Fig. 1. Figure 2 shows a chip photograph. The chip consists of the anode array, the anode selection switches for anode readout, the reference circuit, the charge amplifier (CSA) and its reset

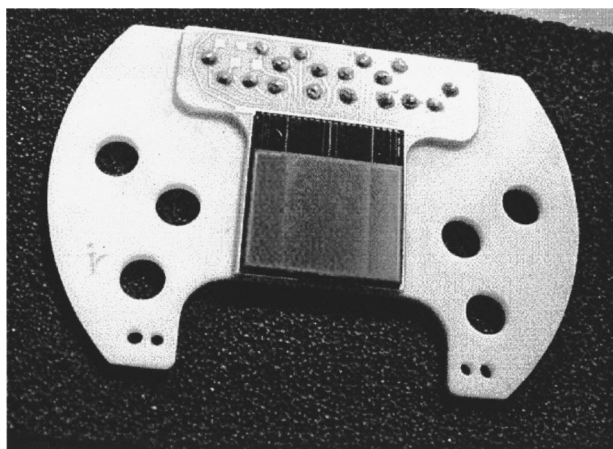


FIG. 2. LEDA512 chip mounted on its ceramic carrier.

circuitry and the digital logic driving the anode selection switches and the reset circuitry. Finally, the output buffers drive the CSA output and the reference voltage off-chip.

The serial read-out of each anode row of the chip is accomplished by means of three digital control lines: clock, start, and reset. The nominal clock speed is 100 kHz so that 10 μ s are available for the read-out of one anode. Figure 3 shows the timing diagram for the digital control lines.

The read-out cycle starts when the shift register in the anode selection logic is reset to its initial conditions. This happens only when the falling edge of *clock* occurs while *start* is high. In all subsequent falling edges of *clock*, *start* is not pulsed high anymore until a new line scan. The shift register selects the first anode of the row after the second falling edge of *clock* and this anode remains selected until the next falling edge of *clock*. During this short period the selected anode is connected to the charge amplifier input and hence is charged to V_{ref} . The charge transferred to the anode is equal to the collected electron charge Q_{in} and charges the feedback capacitor of the CSA. Consequently, the output of the CSA will be

$$V_{out} = V_{ref} + \frac{Q_{in}}{C_f}. \quad (1)$$

After each anode read-out the CSA feedback capacitor must be reset. This is done by means of the reset pulse appearing shortly before the next anode is selected.

The analog output V_{out} corresponding to the charge received by an anode is available at the charge amplifier output after this anode is selected and until *reset* is pulsed high again. The effective output signal is the difference between the V_{out} and V_{ref} . They are both available at the corresponding output pads.

This method of readout has the advantage that the inevitable variations on the anode capacitance between anodes due to process imperfections do not affect the signal. Also, the use of only one CSA instead of one CSA per anode eliminates the effect of gain variations. Hence, there will be no charge-to-voltage conversion nonuniformity due to the LEDA512.

The reason that during the read phase the anode voltage is set to V_{ref} (which is a positive voltage between 2.25 and 2.35 V) is that during charge collection the anode potential drops. Consecutive impacts of ions on the same spectral line will result in charge accumulation on the corresponding anodes. Since the LEDA512 chip is implemented in a CMOS technology compatible with a single 5 V supply, buildup of negative voltages on the anode must be avoided, therefore each anode is precharged to the given positive reference voltage V_{ref} . Electrons collected on an anode will then contribute to the discharge of the anode from this reference level toward the ground reference level.

B. The anode array

In order to choose the width of a single anode, the peak width of the mass peaks produced by the mass spectrometer and the spread of the electron beam at the output of the MCPs must be taken into consideration. Finally, an anode

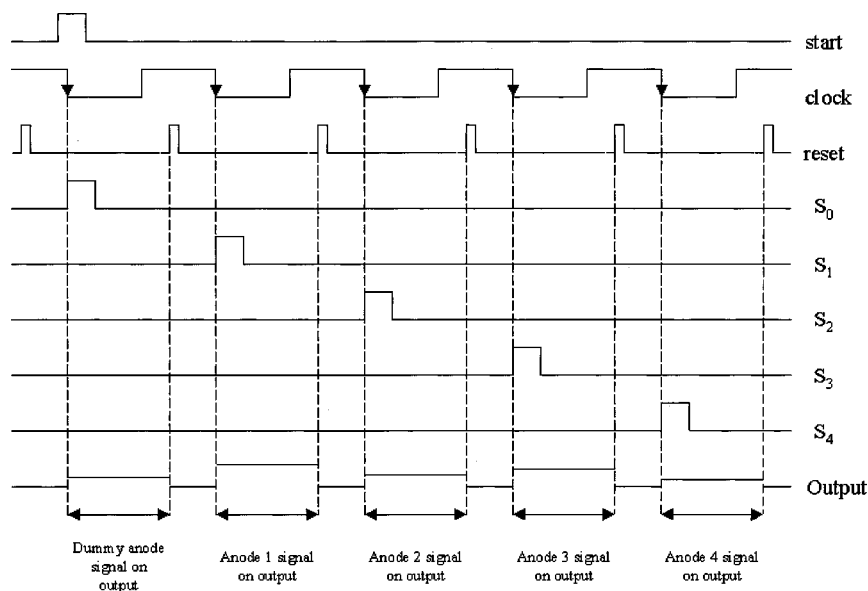


FIG. 3. Timing diagram for the LEDA512 readout.

width of $25\ \mu\text{m}$ was adopted so that a mass peak covers at least six anodes. This would yield a number of anodes around 1000. In practice the number of anodes has been limited to 512 for two reasons: the size limitations imposed by chip manufacturing and the read-out time of the anodes. Each anode was further split in two equal parts, so finally two rows of 512 anodes were obtained. This was required for redundancy reasons as has already been explained. The size of the anodes in the direction perpendicular to the central axis is specified taking into consideration the total height of the spectral lines of the mass spectrometer. This is equal to 16 mm. Since each anode is split into two redundant parts, the anode height becomes 8 mm.

The resulting anode capacitance is 4.22 pF. This value is sufficient to store a charge of 8.44 pC, if we allow the anode voltage to decrease 2 V below the reference level during charge collection. Since a pair of standard MCPs operating at the high end of the operating voltage can produce a current of a few nA per anode, this charge value can be accumulated by one anode in a few ms. The value fits very well with the timing requirement of $10\ \mu\text{s}/\text{anode}$, corresponding to 5.12 ms for the complete array of 512 anodes.

The electrostatic discharge (ESD) protection of anodes is an important issue. Each individual anode has its own protection circuit. Although the anode potential can never rise above V_{ref} under normal operating conditions, a normally reverse biased diode is inserted between each anode and the positive supply. This diode clamps the anode voltage to the positive supply voltage and protects the circuits following the anodes against charge buildup caused by manipulation or leakage currents to or from parts in the neighborhood of the detector. The ESD protection circuits also include a metal-oxide-semiconductor (MOS) transistor-based voltage clamp circuit that monitors the voltage difference between each anode and ground. A transistor having its source connected to the anode is normally nonconducting as long as the voltage level on the anode remains at least 300 mV above ground. If the anode is further discharged, due to (for example) a very intensive mass peak, the transistor starts conducting and

positive charge is injected, which compensates the excess electron input. The current that may be injected is limited to $3\ \mu\text{A}$. This solution is preferred with respect to a simple protection diode connected to ground, because a diode would inject excess charge into the substrate, thus provoking leakage effects in neighboring structures. The complete ESD circuit is shown in Fig. 4.

The influence of the protection circuit on the anode array is minor. The leakage current introduced by these circuits is insignificant compared to the charge arriving from the MCPs. The impact on the anode capacitance may also be disregarded since the protection circuit introduces an extra load of only 5 fF/anode, and consequently a total load of 2.6 pF is added.

The leakage effect on a floating (nonselected) anode is always present but contributes less than 2 pA at room temperature. The total leakage current toward the selected anode is estimated to be 511 times this value. However, it can only influence the anode charge while the anode is being connected. Because the connection time is $10\ \mu\text{s}/\text{anode}$, the effect reduces to an infinitesimally small charge value (approximately 0.02 fC or 2.37 ppm of full scale).

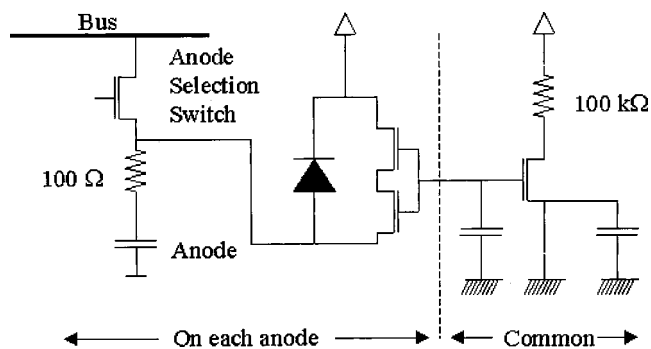


FIG. 4. The electrostatic discharge protection circuit. The left part is repeated for each anode; the right part is common for the whole anode array.

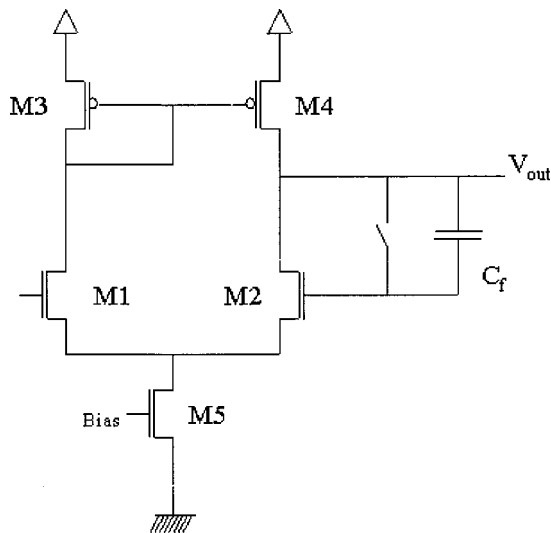


FIG. 5. Schematic of the CSA.

C. Anode selection switches and associated logic

Each of the 512 floating anodes is connected to the charge amplifier input only during a short period of time for read-out and precharge. This connection is accomplished by means of 512 anode selection switches, forming a 512-to-1 multiplexer. The control of these switches is performed by means of a shift register. The total loading of the bus due to the selection switches is estimated as 1.4 pF. As a result, the total loading of the bus due to the switches and the ESD protection circuits is 4 pF.

D. Charge amplifier and unity gain buffers

A common bus line connects the selected anode with the inverting input of the CSA. The feedback capacitance has a value of 6 pF and is realized as a polysilicon to *n*-well capacitor. Figure 5 shows the schematic of this unit. A simple differential pair with *n*-type MOS field effect transistors as input transistors is used for the implementation of the operational amplifier.

The amplifier output, as well as the reference voltage, is driven off-chip by two unity gain buffers. They are implemented using the same differential pair as in the CSA, having the inverting input connected to the output.

E. External connections and shielding

The bonding pads are positioned on a single line along the chip border. This bonding area is displaced by 5 mm, so that a safe distance is created between the pads and the active area where the charge collection is performed. This is necessary in order to avoid contact between bonding wires and the back side of the MCPs. Additionally, a metal shielding layer forms a conducting ring around the anode area. It has a width of 600 μm on the three sides and 400 μm on the bonding side. It is implemented using the same metal layer as the anodes. A separate bonding pad is connected to this ring so that its voltage is kept constant by external circuitry.

III. NOISE CONSIDERATIONS

The data from the LEDA512 chip are fed to a 12-bit analog to digital converter (ADC). The maximum voltage swing in the anodes of 2 V means that a maximum charge of 8.44 pC can be stored. The quantization noise [1 least significant bit (LSB) of the ADC] is therefore equal to roughly 13 000 *e*⁻ rms and is considered as the maximum acceptable noise originating from the chip output.

The readout of the anodes involves the resetting of capacitances and the redistribution of charges. These processes introduce noise together with the noise originating from the CSA. The rest of the anodes at the beginning of the integration time introduces an uncertainty of *Q*_{*n*1} (expressed in number of electrons)

$$Q_{n1} = \sqrt{kTC_d} = 812 e^- \text{ rms}, \tag{2}$$

where *k* is the Boltzmann constant, *T* the absolute temperature, and *C*_{*d*} the anode capacitance. When the signal is being read, the charge is redistributed over the bus capacitance, *C*_{*bus*}. However, this capacitance has been charged before to a level (*V*_{*ref*}) that is also subjected to switching noise. Therefore, the second source of uncertainty introduces

$$Q_{n2} = \sqrt{kTC_{bus}} = 790 e^- \text{ rms}. \tag{3}$$

The CSA itself also introduces noise. If *V*_{*n*} is the total rms input-referred noise integrated over the CSA bandwidth (100 kHz), the CSA contributes with

$$Q_{n3} = C_f V_n. \tag{4}$$

The input referred noise of the CSA can be calculated from the transistor parameters and it is found as 18 μV. Therefore,

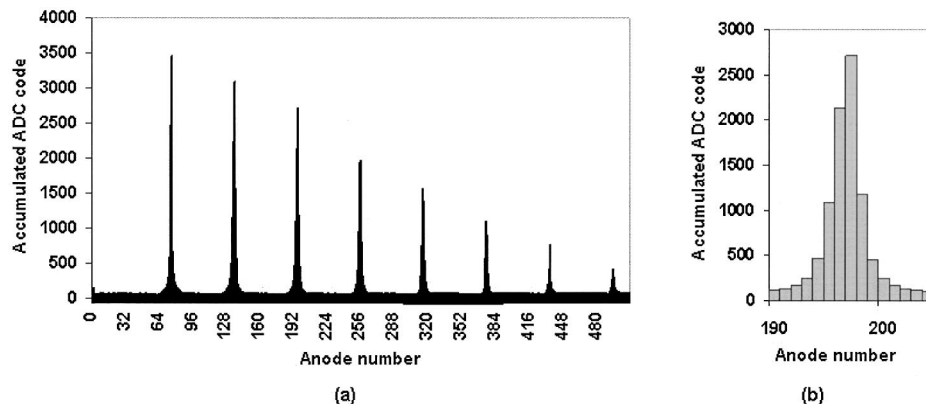


FIG. 6. Simulated spectrum obtained in a vacuum test facility with the LEDA512 prototype, one MCP, and a series of slits of ten micrometer width: (a) the overall response on one row, (b) detail of the peak around anode 197.

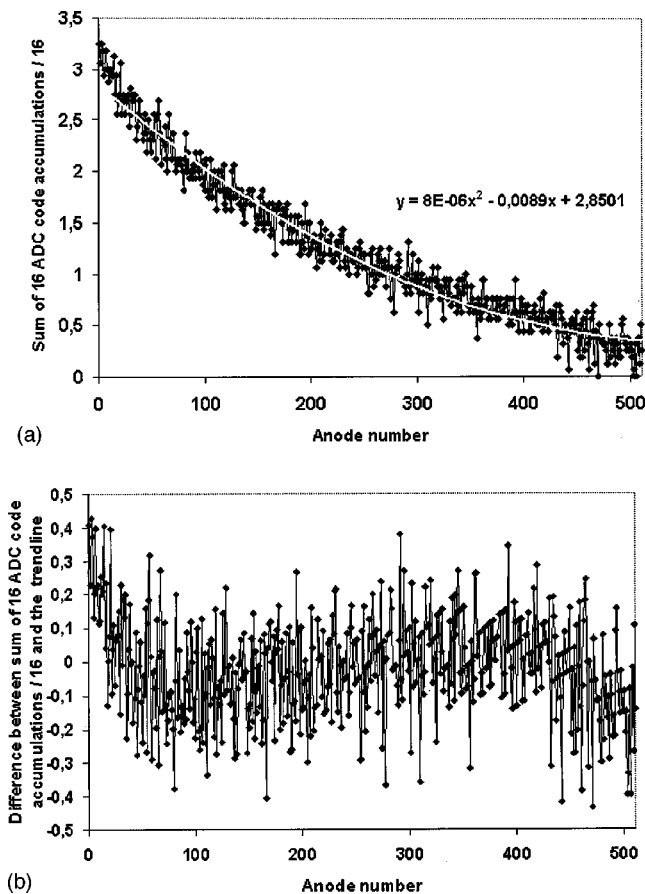


FIG. 7. System noise (LEDA512+MCPs+DFMS): (a) noise+trendline; (b) the remaining noise.

the contribution of the CSA in the total noise is $675 e^-$ rms. The total noise due to internal noise sources is found from

$$Q_n = \sqrt{Q_{n1}^2 + Q_{n2}^2 + Q_{n3}^2} \approx 1300 e^- \text{ rms.} \quad (5)$$

This value is fairly small compared with our requirements. Therefore, there is no need for more complicated readout schemes that suppress noise, as for example correlated double sampling.

IV. MEASUREMENTS

The LEDA512 chip has been subjected to a sequence of tests to verify its performance. The first test was to prove the operational concept. A prototype detector assembly was built for that purpose by BIRA-IASB and our colleagues from CETP-IPSL (St. Maur, France). It consisted of the LEDA512 and a single MCP. The front side of the MCP was covered with a metal shield perforated by means of a number of slits, having a nominal width of $10 \mu\text{m}$ and a length less than the anode height. The slits were positioned in parallel with the anodes and were used to simulate spectral lines of comparable width. Figure 6(a) shows the first, nonoptimized results obtained with this setup in a vacuum test facility equipped with an ion source producing a nonuniform ion beam. Figure 6(b) provides some detail around anode No. 197.

Subsequently, tests were performed with a complete detector assembly consisting of a LEDA512 positioned behind a stack of two MCPs. Figure 7 depicts the result of a mea-

surement wherein 16 background read-outs of the LEDA512 were summed. The resulting response, which is scaled to one read-out and hence represents the mean background, shows a trendline and superimposed noise. At the moment the cause of the monitor trendline effect ($<0.1\%$ of full scale) is not understood. However, when the trend is subtracted the remaining total noise is within ± 0.5 LSB of the ADC, which proves that indeed total system noise, including noise generated by the MCP and the LEDA512 and the associated electronics, is under these conditions less than the quantization noise.

More detailed test results will be published in a subsequent article focused on the complete ROSINA DFMS detector system, which consists of the described LEDA512 chip in combination with an MCP stack and of a Faraday cup and a Channeltron detector, all mounted on a custom made flange.

V. DISCUSSION

It has been demonstrated that a fully redundant anode array consisting of 512 anodes may be built in a commercial CMOS process. The specifications with respect to noise, dynamic range, and read-out speed have been met and the result is an electron detector array that has found its first application in the focal plane detector system for the DFMS mass spectrometer for the ESA ROSETTA cornerstone mission.

Obviously, it may be envisaged to extend the usage of this analog detector chip, based on LEDA512 technology or a derived configuration, to other measurement techniques. Potential fields of application are: staggered configurations of multiple LEDA512 like devices to form longer detector arrays for mass spectrometer focal plane arrays, detection of charged particles filtered by electron or ion energy analyzers, and optical arrays such as a variable gain ultraviolet (UV) sensitive linear array constructed by combining the LEDA512 with a UV sensitive MCP.

In the future, developments for the LEDA512 will be continued in order to integrate more external electronics (amplifiers, ADCs, and logic circuitry) on the chip carrying ceramics. Furthermore, tolerance to space radiation will be improved by using majority logic and radiation tolerant MOS transistors. Finally, an attempt will be made to construct suspended and profile-shaped anodes, which would further reduce current leakage and the escape of secondary electrons.

ACKNOWLEDGMENTS

The authors would like to thank the Belgian Federal Office for Scientific, Technical and Cultural Affairs (DWTC-SSTC) for approval of the ROSINA space project. This work was supported by means of two contracts granted to BIRA-IASB and to IMEC by the European Space Agency PRODEX Office. Furthermore the authors would like to acknowledge the scientific and technical collaborators of the ROSINA teams at BIRA-IASB, at CETP-IPSL, St. Maur, France and at the Physikalisches Institut, University of Bern, Switzerland, for their valuable assistance during the definition and specification phase of the chip and during performance tests.

- ¹G. Schwehm and R. Schulz, *Space Sci. Rev.* **90**, 313 (1999).
- ²H. Balsiger *et al.*, ESA Monograph (in press).
- ³K. Birkinshaw and D. P. Langstaff, *Int. J. Mass Spectrom. Ion Processes* **132**, 193 (1994).
- ⁴M. Lampton and F. Paresce, *Rev. Sci. Instrum.* **45**, 1098 (1974).
- ⁵R. W. Wijngaendts van Resandt, H. C. den Harink, and J. Los, *J. Phys. E* **9**, 503 (1976).
- ⁶P. J. C. M. Nowak, H. H. Holsboer, W. Heubers, and R. W. Wijngaendts van Resandt, *Int. J. Mass Spectrom. Ion Phys.* **34**, 375 (1980).
- ⁷W. Parkes, K. D. Evans, and E. Mathieson, *Nucl. Instrum. Methods* **121**, 151 (1974).
- ⁸D. Krankowsky *et al.*, The Giotto Neutral Mass Spectrometer, Report No. ESA SP-1077, p. 109 (1986).
- ⁹K. Birkinshaw, *Int. Rev. Phys. Chem.* **15**, 1 (1996); **15**, 13 (1996).